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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,271	11/04/2003	Weishi Feng	MP0273	4998

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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,271	FENG ET AL.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 23-33* is/are pending in the application.

4a) Of the above claim(s) *12-22 and 34-59* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 23-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/01/05*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *09/18/06* .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election / Restriction

Restriction to one of the following invention is required under 35 U.S.C. 121

Group I.

Claims 1-11 and 23-33, drawn to a communications channel that receives a user data sequence including N symbols and that supports host CRC, comprising: a host bus interface (HBI) that generates cyclic redundancy check (CRCu) bits based on said user data sequence; and a data dependent scrambler (DDS) that receives said user data sequence and said CRCu bits, that generates a scrambling seed that generates a scrambled user data sequence based on said user data sequence and said scrambling seed, and that generates a difference sequence circuit (as in claim 1) and a communications channel that receives a user data sequence including N symbols and that supports host CRC, comprising: interface means for generating cyclic redundancy check (CRCu) bits based on said user data sequence; and scrambling means for receiving said user data sequence and said CRCu bits, for generating a scrambling seed, for generating a scrambled user data sequence that is based on said user data sequence and said scrambling seed, and for generating a difference sequence (as in claim 22) classified in 714/758.

Group II.

Claims 12-22 and 34-59, drawn a data dependent scrambler for a communications channel that receives a user data sequence including N symbols and host cyclic redundant check (CRCu) bits, comprising: a data buffer that receives said user data sequence and said host CRCu bits; a seed finder that generates a scrambling seed that is dependent upon said symbols in said user data sequence; a first scrambler that receives said user data sequence from said data buffer and said scrambling seed from said seed finder and that generates said scrambled user data sequence; are a second scrambler that generates a difference sequence that is based on said user data sequence and said scrambled user data sequence (as in claim 12) and a data dependent scrambler for a communications channel that receives a user data sequence including N symbols and host cyclic redundancy check (CRCu) bits, comprising: buffer means for storing said user data sequence and said host CRCu bits; seed finding means for generating a scrambling seed that is dependent upon said symbols in said user data sequence; first scrambling means that receives said user data sequence from said data buffer and said scrambling seed from said seed finder for generating said scrambled user data sequence; and second scrambling means for generating a difference sequence that is based on said user data sequence and said scrambled user data sequence (as in claim 34) classified in 714/7.

The invention are distinct, each from the other because of the following reasons:

Invention Group I and group II are related as subcombinations disclosed **as usable together in a single combination.** The subcombinations are distinct from each other if they are shown to be separately usable.

In the instance case, the invention Group I is a host bus interface (HBI) or an interface means that generates cyclic redundancy check (CRCu) bits based on said user data sequence; and a data dependent scrambler (DDS) that receives said user data sequence and said CRCu bits, that generates a scrambling seed that generates a scrambled user data sequence based on said user data sequence and said scrambling seed, and that generates a difference sequence circuit.

In the instant case, the invention Group II is a host bus interface (HBI) or an interface means that generates cyclic redundancy check (CRCu) bits based on said user data sequence; and a data dependent scrambler (DDS) that receives said user data sequence and said CRCu bits, that generates a scrambling seed that generates a scrambled user data sequence based on said user data sequence and said scrambling seed, and that generates a difference sequence circuit.

Because these inventions are distinct for the reason given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and the reasons given above and search required for Group II is not for Group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Attorney Michael Wiggins on 18 september 2006 a provisional election was made with traverse / without traverse to prosecute the invention of Group I, claims 1-11 and 23-33.

DETAILED ACTION

1. Claims **1-11 and 23-33** are presented for examination.

Priority

2. Acknowledgment is made of applicant's claim for domestic priority under 35 U.S.C. 119 (e) (provisional application #60/442,956) filed on 01/27/2003.

Information Disclosure Statement

3. The references listed in the information disclosure statement submitted on 02/01/05 have been considered by the examiner (see attached PTO-1449).

Specification

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim objections

5. Claims **1 and 23** are objected to because of the following informalities:

a) Please change the paragraph "a data dependent scrambler (DDS) that receives said user data sequence and said CRCu bits, that generates a scrambling seed that generates a scrambling seed that generates a scrambled user data sequence based on said user data sequence and said scrambling seed, and that generates a difference sequence" to ---"a data dependent scrambler (DDS) receives said user data sequence and said CRCu bits and generates a scrambling seed and further generates a scrambled user data sequence based on said user data sequence and said scrambling seed and furthermore generates a difference sequence ---(see lines5-8) (see claims 1 and 23). The examiner suggests if the claims limitation are amended to read as mentioned in the above in order to avoid grammatical problems:

b) Please define the full word of a written word or phrase for the abbreviations "CRC**u**, CRC**d** and CRC**w** " as specified in the specification (see Claims 1-5 and 23-27).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U. S. C 112

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

6. Claims **1 and 23** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a) Claims 1 and 23 recite, "a data dependent scrambler (DDS) receives said user data sequence and said CRCu bits". It is not clear how and from where the DDS receives the user data sequence and CRCu bits. For example, the DDS could receive

the data and the CRC from any means through different channels. The examiner would appreciate if the applicant would clarify this matter.

Claims 1 and 23 recite, "generates a scrambled user data sequence based on the user data sequence and the scrambling seed and generates a difference sequence". It is not clear how the scrambled user data sequence is affected by the user data sequence and the scrambling seed and further generates a difference sequence. For example, the scrambled user data sequence could be generated only if user data sequence and the scrambling seed satisfy certain conditions. The examiner would again appreciate if the applicant would clarify this matter.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claim **1-5, 9-10, 23-27 and 30-32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama et al. (U.S. Pub. No: US2003/0135798).

As per claims 1-4:

Katayama et al. in figure 3 or figure 17 substantially teach or disclose a host interface (HOST I/F) (311) controls data transfer between the optical disk device and a host computer coupled to a scramble circuit (309) (data dependent scrambler) and randomizes data and the scrambled data further coupled to an error correction coding circuit (307) adds an error correction code to the randomized data and a run limit length coding circuit (305) modulates the data added with the error correcting code in accordance with the rule determined in advance and converted the modulated data to be recorded to an optical disk (301) a recorded medium (see page 4 paragraph [0078]) and further the obtained data is demodulated in a run length limit code decoding circuit (305) coupled to an error correcting circuit (308) to calculate an error position and an error value on the basis of error correcting code added by the error correction coding circuit (307) and the error are corrected (see col.5 paragraph [0079]). Furthermore, Katamaya et al. teach a seed generator (see figure 14, 2603) for giving a different seed to the random seed scrambler within the scrambler (2601) wherein the scrambler coupled to the error correcting circuit (see page 6 paragraph [0105]). **It is noted, however**, Katamaya et al. **do not explicitly detail** the aspects of "a host bus interface generates a CRC" as recited in claims 1 and 22. **On the other hand,** Katayama et al. teach that a user data (see figure 11, 1101) of 2048 bytes are inputted from the interface (311) (see figure 15, step 1501) and in the ID adder (see figure 14, 1401) and error detection code (EDC) (see figure 11, 1107) of four bytes added to the user data (1101) inputted form the interface (311) (see col. 7 paragraph [0109]) which Katayama basically the same as the applicant's invention or referring to a general error detection

codes (EDC) including CRC codes for checking of detecting errors. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to follow the steps and the connection between the elements (host, scrambler, ECC circuit) mentioned in the above to scramble and detect/correct data. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would be relatively and yet high reliable in operation.

As per claims 5 and 27:

Katayama et al. in figure 3 substantially teach or disclose a run limit length (RLL) coding circuit (305) modulates the data added with the error correcting code in accordance with the rule determined in advance and converted the modulated data to be recorded to an optical disk (301) a recorded medium (see page 4 paragraph [0078]) and further the obtained data is demodulated in a run length limit code decoding circuit (305) coupled to an error correcting circuit (308) to calculate an error position and an error value on the basis of error correcting code added by the error correction coding circuit (307) and the error are corrected (see col.5 paragraph [0079]).

As per claims 6-8:

Katamaya et al. in figure 14 disclosed an interface (311) coupled to a seed generator (2603) for giving a different seed to the random seed scrambler within the scrambler (2601) wherein the scrambler coupled to the error the a RAM (buffer) (1402) through an error correcting circuit (307) (see page 6 paragraph [0105]).

As per claims 9 and 31:

Katamaya et al. teach a technique that provides a scramble coding-decoding method to be executed in a memory device for recording data to a rewritable memory medium and regenerating the data from memory medium, and its circuit (see col. 2 paragraph [0012 and 0013]).

As per claims 10 and 32:

Katamaya et al. in figure 55 a block diagram of scrambling coding circuit constructed by one XOR circuit (4177) and M-bit memories (see page 21, paragraph [0214]).

As per claims 23-26:

Katayama et al. in figure 3 or figure 17 substantially teach or disclose a host interface (HOST I/F) (311) controls data transfer between the optical disk device and a host computer coupled to a scramble circuit (309) (data dependent scrambler) and randomizes data and the scrambled data further coupled to an error correction coding circuit (307) adds an error correction code to the randomized data and a run limit length coding circuit (305) modulates the data added with the error correcting code in accordance with the rule determined in advance and converted the modulated data to be recorded to an optical disk (301) a recorded medium (see page 4 paragraph [0078]) and further the obtained data is demodulated in a run length limit code decoding circuit (305) coupled to an error correcting circuit (308) to calculate an error position and an error value on the basis of error correcting code added by the error correction coding circuit (307) and the error are corrected (see col.5 paragraph [0079]). Furthermore, Katamaya et al. teach a seed generator (see figure 14, 2603) for giving a different seed

to the random seed scrambler within the scrambler (2601) wherein the scrambler coupled to the error correcting circuit (see page 6 paragraph [0105]). **It is noted, however**, Katamaya et al. **do not explicitly detail** the aspects of "a host bus interface generating a CRC" as recited in claims 1 and 22. **On the other hand,** Katayama et al. teach that a user data (see figure 11, 1101) of 2048 bytes are inputted from the interface (311) (see figure 15, step 1501) and in the ID adder (see figure 14, 1401) and error detection code (EDC) (see figure 11, 1107) of four bytes added to the user data (1101) inputted form the interface (311) (see col. 7 paragraph [0109]) which Katayama basically the same as the applicant's invention or referring to a general error detection codes (EDC) including CRC codes for checking of detecting errors. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to follow the steps and the connection between the elements (host, scrambler, ECC circuit) mentioned in the above to scramble and detect/correct data. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would be relatively and yet high reliable in

As per claims 28-30:

Katamaya et al. in figure 14 disclosed an interface (311) coupled to a seed generator (2603) for giving a different seed to the random seed scrambler within the scrambler (2601) wherein the scrambler coupled to the error the a RAM (buffer) (1402) through an error correcting circuit (307) (see page 6 paragraph [0105]).

8. Claims **11 and 33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama et al. (U.S. Pub. No: US2003/0135798) in view of Applicants' admitted prior art.

As per claims 11 and 33:

Katamaya et al. teach all the subject matter claimed in claims 1 and 22. Katamaya et al. do not explicilty teach a buffer manager, a buffer and a disk formatter located between said the HBI and the DDS. **However,** the Applicants' admitted prior art figure 2 disclose buffer manager, a buffer and disk formatter coupled to each other between the HBI and scrambler. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to incorporate the elements of Applicants' admitted prior art in the art of Katayama et al. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would enhance the accuracy of the decoding process and the overall system performance.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,671,832

US PN: 6,618,395

US PN: 7,082,258

US PN: 6,738,953

US PN: 6,850,499

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Art unit: 2133

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